Beijing Converters: Bridge Converters with a Capacitor Added to Reduce Leakage Currents, DC-Bus Voltage Ripples and Total Capacitance Required

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***Abstract*—Isolation transformers and bulky electrolytic capacitors are often used in power electronic converters to reduce leakage currents and voltage ripples but this leads to low power density and reduced reliability. In this paper, an auxiliary capacitor is added to the widely-used conventional full-bridge converter to provide a path for, and hence significantly reduce, the leakage current. The operation of the full-bridge converter is split into the operation of a half-bridge converter and a DC-DC converter so that the ripple energy can be diverted from the DC-bus capacitor to the auxiliary capacitor. Hence, the DC-bus capacitor can be significantly reduced while maintaining very low voltage ripples on the DC bus because it is only required to filter out switching ripples. The auxiliary capacitor is designed to allow high voltage ripples because its voltage is not supplied to any load. Accordingly, the auxiliary capacitor can also be very small as well. As a result, the total required capacitance becomes very small. The reduction ratio of the total capacitance is significant, which makes it cost-effective to use film capacitors instead of electrolytic capacitors. The proposed converters can be also operated as an inverter without any restriction on power factor because the adopted four switches are all bidirectional in terms of power flow. Experimental results for both rectification and inversion modes are presented to demonstrate the performance of the proposed converter in reducing the ripples, the leakage currents and the total capacitance needed, with comparison to the conventional bridge converter without the auxiliary capacitor.**

***Index Terms*—Voltage ripples, electrolytic capacitors, common mode (CM), leakage currents, transformerless, bridge converters, neutral leg.**

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I. Introduction

POWER electronic converters are widely used to convert AC voltages into DC voltages or DC voltages to AC voltages. There are numerous kinds of topologies for such converters [1], among which the conventional full-bridge converter with four active switches is one of most popular topologies. Full-bridge converters often need an isolation transformer, at either high or low frequencies, to cut off the current path of leakage currents in order to avoid electric shock and to reduce EMI [2]. However, isolation transformers lead to low power density and reduced power efficiency [2]. Moreover, converters often need bulky electrolytic capacitors to smooth the pulsating power, in particular, for single-phase systems [3]. However, it is well known that the reliability of electrolytic capacitors can be a serious problem and almost one third of failures for power electronic systems are due to the failure of electrolytic capacitors [4].

The reduction of the leakage current for the full-bridge converter can be achieved by either reducing the common mode (CM) voltage or increasing the CM impedance. If the bipolar sinusoidal pulse width modulation (SPWM) is applied to the full-bridge converter, then the voltage across parasitic capacitors is clamped at half of the DC-bus voltage. However, the system performance is degraded in terms of grid current ripples and switching losses [5]. It is even possible to further reduce the voltage from half of the DC-bus voltage to zero if both DC and the AC grounds are connected together, as reported in [5]. The reduction of the CM voltage can be also achieved by decoupling AC and DC sides of converters during freewheeling phases [6], [7] and changing the modulation strategies [8]. Although the above methods can reduce the leakage current, they have an increased number of switches and suffer from reduced ability to process reactive power [2], [5] and/or degraded performance caused by modulation strategies and/or parasitic capacitors of switches [5].

The reduction of the leakage current can also be achieved by increasing the impedance on the path of the leakage current, e.g. by adopting CM filters [9] or using isolation transformers. However, this reduces the power density because of the large size and heavy weight of the CM filters and the isolation transformers. The effectiveness of such impedance may be seriously deteriorated by parasitic parameters. For

example, inter-winding capacitance of isolation transformers can significantly decrease the impedance between the primary and secondary sides of transformers, which, in return, leads to degraded performance on the reduction of leakage currents [10]. Shielding is widely adopted to reduce effective parasitic capacitances associated with the most severe voltage pulsating nodes [10]. However, the inserted shielding layers inevitably result in increased size, cost and power loss of transformers.

The reduction of the usage of electrolytic capacitors has become a hot topic during the last few years. In general, the reduction can be achieved by either reducing the system ripple energy or providing another buffer with high allowable voltage ripples to store the ripple energy. The first approach was achieved by injecting third and/or fifth harmonic into the grid current [11]. This can be very cost-effective because no auxiliary circuits or power components are needed while the only compromise is the increased total harmonic distortion (THD) and reduced input power factor. The second approach needs active circuits to store the ripple energy so that the ripple energy flowing through the DC-bus capacitors can be reduced or even completely eliminated. The active circuits can be connected in parallel at the DC side [3] or in series with the DC bus at the DC side [12]. Although some of the above solutions are not specially designed for full-bridge converters, it is straightforward to apply these to full-bridge converters. Most of these active circuits are actually DC/DC buck/boost converters with two or more power switches, one inductor and one capacitor so the cost of the system is inevitably increased although the required capacitance is reduced.

In order to achieve high power density and reliability, it is desirable to reduce the leakage current and the total required capacitance at the same time, while achieving the desired voltage ripples. This can be achieved by combining the aforementioned solutions. For example, the series compensator proposed in [12] can be applied to the system proposed in [5]. However, this will inevitably increase the complexity and cost of the system. Instead of such combination of solutions, it is, of course, better to achieve the reduction of both leakage current and capacitance together in a holistic way. For example, the midpoints of a split-phase single-phase system at both the DC and AC sides are constructed and connected together in [13] to eliminate the isolating transformer and bulky electrolytic capacitors with six switches. Another example [14] was reported for asymmetrical single-phase systems, which needs four switches. As a result, two switches are saved compared to the converter in [13]. The only compromise is that the converter presented in [14] needs switches with higher voltage-rating, which leads to increased system costs and losses.

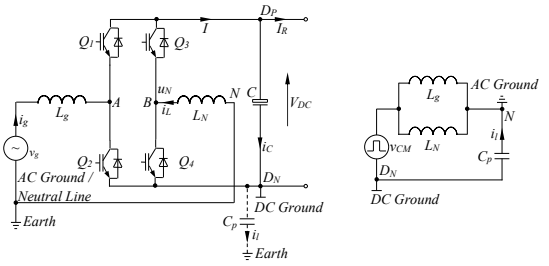
In this paper, the idea of holistically reducing leakage current and capacitance is further explored, following the work in [15]. A simple topological change is proposed to the conventional full-bridge converter via adding a small auxiliary capacitor. The capacitor is connected between the grid neutral line and the negative pole of the DC bus. As a result, the added auxiliary capacitor is actually in parallel with the parasitic capacitors and provides a path for the leakage current. Hence, the leakage current can be considerably reduced without using an isolation transformer. Due to the significantly-reduced leakage current, for applications that still require isolation transformers for safety purpose, the size, cost and power loss of such transformers are reduced because there is no need to insert any shielding layers to reduce inter-winding capacitance [10]. Moreover, the operation of the converter is changed to the independent operation of a half-bridge converter and a DC/DC converter so that the ripple energy originally flowing through the output capacitor is now diverted to the auxiliary capacitor. As a result, the DC-bus capacitance can be significantly reduced. At the same time, the auxiliary capacitor is designed to allow large voltage ripples because no loads are connected to the auxiliary capacitor. Hence, the auxiliary capacitor can be also very small. Hence, the total capacitance required becomes very small and highly-reliable film capacitors instead of electrolytic capacitors can now be used. The proposed converter is mainly for systems without hold-up time requirement. For systems with the hold-up requirement, the required capacitance needs to be large enough if no other means is applied to provide the energy required (see [16] for example).

The impact of adding the auxiliary capacitor with large voltage ripples is analysed in detail. Because the operation of the proposed converter is similar to that of the half-bridge converter, the proposed converter inherits many features of the half-bridge converter, e.g. the same range of the DC output voltage and simple drive circuits. As a result, the proposed converter is suitable for loads that are originally supplied by conventional half-bridge converters. The two legs of the proposed converter are independently controlled so there is no need to synchronise the driving signals for both legs, which simplifies the design of the driver circuits. One leg is responsible for the energy exchange between the AC and DC sides and the other leg is responsible for diverting the ripple energy to the auxiliary capacitor. Note that the converter can be operated in the inversion mode without any restriction on power factor. The functions mentioned above still hold true when the proposed converter is operated as an inverter.

The topology of the proposed converter can also be derived from the topology presented in [14] by changing locations of DC capacitors and load. The number of switches, capacitors and inductors is kept to be the same. However, the voltage rating of switches is lowered for the proposed converter when the DC output voltage of both converters is set at the same value. As a result, the system performance on costs and efficiency can be improved. Compared to [14], the new contributions of this paper include: 1) lowering the voltage rating of switches; 2) analysing the leakage current with comparison to that in conventional full-bridge converters to demonstrate the reduction; 3) proposing control strategies to holistically achieve the reduction of the leakage current and capacitance; 4) demonstration of the operation as an inverter.

II. Conventional Single-phase Full-bridge Converter

The conventional single-phase full-bridge converter is shown in Fig. 1(a), with four power switches connected as two legs. The two switches on each leg are normally operated



(a) (b)

Fig. 1. Conventional single-phase full-bridge converter: (a) topology; (b) equivalent circuit for analysing leakage currents.

complementarily and the two legs are operated complementarily as well. The switches are operated at high frequencies to inject the right amount of current into the DC bus so that the DC-bus voltage is regulated. The power factor of converters is often required to be close to 1. A lot of technologies have been developed to improve the performance of the converter from different aspects such as control strategies, modulation strategies, power density, reliability and efficiency [1], [2].

A. The Need of an Isolation Transformer

The equivalent circuit for analysing the leakage current of the conventional full-bridge converter is shown in Fig. 1(b). The equivalent CM voltage is

$$v_{CM} = \frac{v_{AD_N} + v_{BD_N}}{2} + (v_{AD_N} + v_{BD_N})\frac{L_N - L_g}{L_N + L_g} \quad (1)$$

where v_{AD_N} and v_{BD_N} are the voltages between points A and D_N and between points B and D_N, respectively. The voltages v_{AD_N} and v_{BD_N} depend on both the system parameters and the modulation strategies. Because of the parasitic capacitor C_p between the DC ground and the earth, a current loop is formed and the leakage current i_l appears. The impedance of the CM loop is

$$Z(s) = s\frac{L_N L_g}{L_N + L_g} + \frac{1}{sC_p} \quad (2)$$

from which the leakage current can be found as

$$i_l = \frac{sC_p}{s^2\frac{L_N L_g C_p}{L_N + L_g} + 1} v_{CM}. \quad (3)$$

This leakage current could lead to reduced system efficiency, high electromagnetic emissions and safety issues [2]. In order to limit this current, either a low-frequency or high-frequency isolation transformer is often needed to cut off the path of the i_l by providing a galvanic isolation between the DC side and the AC side of the converter [5]. However, this reduces system efficiency, power density and reliability.

B. The Need of Bulky DC-bus Electrolytic Capacitors

Assume that the grid voltage is

$$v_g = V_g \sin \omega t, \quad (4)$$

where V_g is the peak value of the grid voltage and ω is the angular grid frequency. With the unity power factor, it can be assumed that the grid current is

$$i_g = I_g \sin \omega t, \quad (5)$$

where I_g is the peak value of the grid current. As a result, the instantaneous input power $v_g i_g$ consists of a constant component $\frac{V_g I_g}{2}$ and a ripple component $-\frac{V_g I_g}{2}\cos 2\omega t$. Ideally, the power consumed by the DC load is constant, i.e. $\frac{V_g I_g}{2}$, when ignoring power losses, so an energy buffer is needed to store the ripple component. This is often achieved by using DC capacitors. Assume that all the ripple energy is stored in DC capacitors. Then the required DC capacitance is

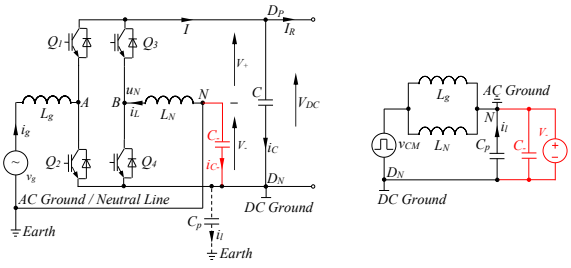
$$\begin{aligned} C &= \frac{V_g I_g}{\omega(V_{DCmax}^2 - V_{DCmin}^2)} \\ &\approx \frac{V_g I_g}{2\omega \triangle V_{DC} V_{DC0}} \end{aligned} \quad (6)$$

where V_{DCmax}, V_{DCmin}, $\triangle V_{DC}$ and V_{DC0} are the maximum, minimum, peak-peak and average values of V_{DC}, respectively. If $\triangle V_{DC}$ is required to be very small, the required capacitor C could be very large, which often reaches a level that only electrolytic capacitors are cost-effective to be used.

III. The Proposed Beijing Converter

A. Topology

The proposed converter is formed by adding a small auxiliary capacitor C_- into the conventional full-bridge converter between the neutral line N and the negative pole D_N of the DC bus, as shown in Fig. 2(a). Moreover, the operation of the bridge converter is changed: Q_1 and Q_2 are operated as a half-bridge converter, called the conversion leg, and Q_3 and Q_4 are operated as a DC/DC converter, called the neutral leg. They share the same neutral point N. Since the used four switches are bidirectional in terms of power flow, the proposed converter can be also operated in the inversion mode without any restriction on the power factor. In order to facilitate the following analysis, the main focus in the sequel will be paid on the rectification mode and similar analysis can be easily applied to the inversion mode with only minor changes.



(a) (b)

Fig. 2. The proposed converter: (a) topology; (b) equivalent circuit for analysing leakage currents.

B. Operation Principle

For conventional full-bridge converters, the two legs are operated in a complementary way [1]. As a result, the control of the two legs are not independent. The main objectives of

the two legs are to regulate the grid current and the DC-bus voltage. Note that the regulation of the DC-bus voltage can be indirectly achieved by injecting the right amount of the grid current. Hence, there is only one independent objective, i.e. the regulation of the grid current.

For the proposed converter, the two legs are operated independently from each other and they can be operated to achieve their own objectives with the corresponding control strategies designed properly. Here, the conversion leg is still used to regulate the grid current and maintain the DC-bus voltage. The neutral leg is used to achieve some other objectives, in addition to providing the return path of the grid current. One option is to divert the ripple energy from the DC bus to the auxiliary capacitor. This can be achieved by complementarily operating the two switches of the neutral leg to absorb/inject the right amount of currents from/to the DC bus and the auxiliary capacitor. In order to make this happen, the average voltage across the auxiliary capacitor V_{-} needs to be regulated within a certain range as well.

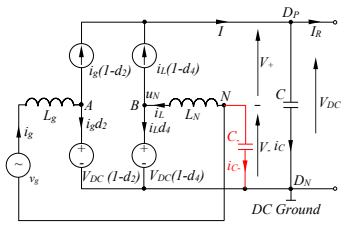


Fig. 3. Average circuit model of the proposed converter.

C. Average Circuit Model

According to [17], the average circuit model of the proposed converter can be built as shown in Fig. 3. As reported in [18], the IGBT switch can be modelled as a static nonlinear system. Here, the system input is the duty cycle of the switch and the output can be the voltage across the switch and/or the current flowing through the switch depending on practical requirements. The voltage/current depends on the value of the system input only at that instant instead of any previous inputs [18]. If the system input contains AC variables, the system output would be a combination of a DC voltage/current, if any, with AC voltages/currents at different frequencies, which can be described by a Taylor series expansion [18]. Here, only low-frequency (e.g., fundamental and second-order) and DC variables are considered because high-frequency ones are normally very small [18]. As a result, for these variables, it is accurate enough to use the averaged variables, e.g., average currents and average voltages, to well represent the original variables according to the averaging theory [19]. In this case, a switch can be modelled as either a voltage source or a current source as needed. However, it is important to mention that the two switches in one leg cannot be modelled as voltage sources at the same time. Otherwise, it is impossible to predict the average currents flowing through individual switches [17]. Similarly, the two switches in one leg cannot be modelled as current sources at the same time.

Based on the above analysis, the switches Q_1 and Q_2 are replaced with a current source $i_g(1-d_2)$ and a voltage source $V_{DC}(1-d_2)$, where d_2 is the duty cycle of Q_2. At the same time, the switches Q_3 and Q_4 are replaced with a current source $i_L(1-d_4)$ and a voltage source $V_{DC}(1-d_4)$, where d_4 is the duty cycle of Q_4. Because the switching frequency is much higher than the line frequency, there are

$$v_g = V_{DC}(1-d_2) - V_{-} \quad (7)$$

$$V_{-} = V_{DC}(1-d_4). \quad (8)$$

As a result, the duty cycles of the Switch Q_2 and the Switch Q_4 can be found as

$$d_2 = \frac{V_{+}}{V_{DC}} - \frac{V_g}{V_{DC}}\sin\omega t \quad (9)$$

$$d_4 = \frac{V_{+}}{V_{DC}} = 1 - \frac{V_{-}}{V_{DC}}. \quad (10)$$

D. Reduction of the DC-bus Voltage Ripples

According to the Kirchhoff's law, there are

$$i_C = i_g(1-d_2) + i_L(1-d_4) - I_R \quad (11)$$

$$i_{C-} = -i_g - i_L = -I_g\sin\omega t - i_L \quad (12)$$

where i_C, i_{C-} and I_R are the currents flowing through the capacitor C, the capacitor C_{-} and the load, respectively, ignoring the switching-frequency components. Moreover, if the power losses are neglected, then the DC load current is

$$I_R = \frac{V_g I_g}{2V_{DC}} \quad (13)$$

because of power balance. Substituting (9)-(10) into (11), then

$$i_C = \frac{V_{-}I_g}{V_{DC}}\sin\omega t - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t + \frac{V_{-}}{V_{DC}}i_L \quad (14)$$

where i_L is the current of the inductor L_N. Both capacitor currents could contain fundamental, second-order and other frequency components, which lead to voltage ripples across the capacitors C and C_{-} if not controlled properly.

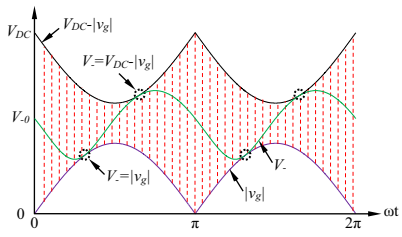


Fig. 4. Range of the voltage V_{-} determined by $|v_g|$ and $V_{DC}-|v_g|$.

In order to divert the ripple energy away from the capacitor C, it is required to force $i_C = 0$, or

$$i_C = \frac{V_{-}I_g}{V_{DC}}\sin\omega t - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t + \frac{V_{-}}{V_{DC}}i_L = 0. \quad (15)$$

The current flowing through the inductor L_N should be

$$i_L = -I_g\sin\omega t + \frac{V_g I_g}{2V_{-}}\cos 2\omega t. \quad (16)$$

Substituting (16) into (12), the current flowing through the capacitor C_{-} becomes

$$i_{C-} = -\frac{V_g I_g}{2V_{-}}\cos 2\omega t, \quad (17)$$

which means the current i_{C-} mainly contains a second-order component. Because the voltage across the capacitor C_- is not connected to any load, it could be designed to have large voltage ripples with a small capacitor. Since i_C does not contain any low frequency currents, the capacitor C can be significantly reduced while still maintaining low voltage ripples. Although an auxiliary capacitor (C_-) is added, the total capacitance $C + C_-$ could still be reduced considerably.

E. Operational Boundary

Because the voltage V_- and the current i_{C-} satisfy

$$i_{C-} = C_- \frac{dV_-}{dt}, \tag{18}$$

according to (17), there is

$$2V_- \frac{dV_-}{dt} = -\frac{V_g I_g}{C_-} \cos 2\omega t. \tag{19}$$

As a result,

$$V_-^2 = V_{-0}^2 - \frac{V_g I_g}{2\omega C_-} \sin 2\omega t, \tag{20}$$

where V_{-0} is the DC component of V_-. In order to ensure the boost operation of the converter, both $V_+ = V_{DC} - V_-$ and V_- should not be lower than the grid voltage. In other words, it is required that

$$V_{DC} - |V_g \sin \omega t| \geqslant V_- \geqslant |V_g \sin \omega t|, \tag{21}$$

as shown in the shaded area in Fig. 4. In the extreme case, the waveform of the voltage V_- is tangent to the waveforms of both $V_{DC} - |V_g \sin \omega t|$ and $|V_g \sin \omega t|$, and the voltage V_- achieves the maximum allowed ripples and the capacitor C_- achieves its minimum value according to (20).

Since $V_- \geqslant |V_g \sin \omega t|$, there is

$$V_-^2 \geqslant V_g^2 \sin^2 \omega t, \tag{22}$$

which means, according to (20),

$$\begin{aligned} V_{-0}^2 - \frac{V_g^2}{2} &\geqslant -\frac{V_g^2}{2} \cos 2\omega t + \frac{V_g I_g}{2\omega C_-} \sin 2\omega t \\ &= \lambda \sin(2\omega t - \arccos(\frac{V_g I_g}{2\lambda \omega C_-})) \end{aligned} \tag{23}$$

with

$$\lambda = \sqrt{(\frac{V_g I_g}{2\omega C_-})^2 + (\frac{V_g^2}{2})^2}. \tag{24}$$

As long as the system parameters are determined, the left part of (23), i.e. $V_{-0}^2 - \frac{V_g^2}{2}$, is determined. Note that the right part of (23) is time-varying at the second-order frequency. In order to make sure that (23) is always satisfied, the minimum value $V_{-0_{min}}$ of V_{-0} should satisfy

$$V_{-0_{min}}^2 - \frac{V_g^2}{2} = \sqrt{(\frac{V_g I_g}{2\omega C_-})^2 + (\frac{V_g^2}{2})^2}. \tag{25}$$

According to (20) and (25), the operation boundary of the minimum value of V_- can be found as

$$V_{-bmin} = \sqrt{\frac{V_g^2}{2} + \frac{V_g^2}{2}(\sqrt{\frac{(\frac{I_g}{\omega C_-})^2}{V_g^2} + 1} - \frac{\frac{I_g}{\omega C_-}}{V_g})}, \tag{26}$$

which belongs to $[\frac{V_g}{\sqrt{2}}, V_g)$, and the operation boundary of the maximum value of V_- can be found as

$$V_{-bmax} = \sqrt{\frac{V_g^2}{2} + \frac{V_g^2}{2}(\sqrt{\frac{(\frac{I_g}{\omega C_-})^2}{V_g^2} + 1} + \frac{\frac{I_g}{\omega C_-}}{V_g})}. \tag{27}$$

In practice, V_{-bmin} is often close to the RMS grid voltage $\frac{V_g}{\sqrt{2}}$. For a tentatively chosen C_-, the minimum and maximum values of V_- can be determined according to (26) and (27). If the resulting V_- exceeds $V_{DC} - |V_g \sin \omega t|$, then the maximum value of the V_- should be decreased by increasing the capacitor C_- until it is satisfied. In this way, the capacitor C_- can be determined, together with the range of V_-.

F. Reduction of the leakage Current

The equivalent circuit for analysing the leakage current is shown in Fig. 2(b). Because the capacitor C_- is connected in parallel with the parasitic capacitor C_p, the voltage across the parasitic capacitor is clamped to the voltage V_- and the resulting leakage current is

$$i_l = sC_p V_-, \tag{28}$$

which is significantly reduced with comparison to the original leakage current (3) because V_- is designed to contain a DC component and a second-order ripple, which do not make much contribution to the leakage current, plus a switching ripple, which is designed to be small. Hence, an isolation transformer is no longer needed. Importantly, the reduction of the i_l is achieved naturally without any additional effort.

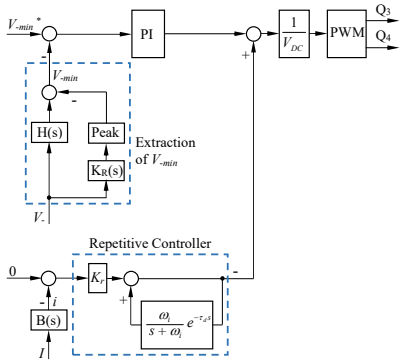


Fig. 5. Controller for the neutral leg.

IV. Control Design

As mentioned before, the control of the two legs is independent from each other. The main objective of the conversion leg is to regulate the DC-bus voltage via controlling the grid current to be in phase with the grid voltage so that the unity power factor can be achieved as well. The control of the conversion leg is very similar to that of conventional half-bridge and full-bridge converters and the detailed control structure is not given here because of the page limit. Interested readers are referred to [1], [14]. The following design is focused on the controller for the neutral leg. The main objective of the neutral leg is to divert the ripple energy from the DC bus to the capacitor C_-, or in other words, to make the current flowing through the capacitor C to be zero. This can be achieved by making the non-DC component of the current I to be zero.

A. Regulation of the DC Component of V_-

According to (10), the regulation of V_- can be achieved by changing the duty cycle d_4. This can be achieved by controlling the average, minimum or maximum value of the voltage V_-. In this paper, the control objective is set to control the minimum value of the voltage V_- at a given value, denoted as V_{-min}^*. For this purpose, the minimum value of the voltage V_-, denoted as V_{-min}, is extracted by using the average voltage to subtract the peak value of the voltage ripple $\triangle V_-$. The average voltage can be obtained by using the hold filter

$$H(s) = \frac{1 - e^{-Ts}}{Ts} \tag{29}$$

where T is the fundamental period of the grid voltage, as shown in Fig. 5. At the same time, the measured voltage V_- is sent to the following resonant filter

$$K_R(s) = \frac{K_h 2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2} \tag{30}$$

to extract the $\triangle V_-$. The filter is tuned at the second-order harmonics with $\omega = 2\pi f$, $K_h = 1$, $\xi = 0.01$ and $h = 2$, where $f = 50\,\text{Hz}$ is the system fundamental frequency. Then, the peak value of $\triangle V_-$ can be extracted by squaring the $\triangle V_-$ with the result sent to a hold filter. Once the minimum value of the voltage V_- is obtained, a simple proportional-integral (PI) controller can be adopted to regulate it at the given value via generating the right duty cycle d_4.

B. Removal of Low-Frequency Ripples from V_{DC}

In order to make the DC-bus voltage ripple-free, all the low frequency ripples should be removed from the current i_C. This can be achieved by making the DC-bus current I ripple-free. The low-frequency component of the DC-bus current I can be extracted with a bandpass filter, e.g.

$$B(s) = \frac{10000s}{(s+10)(s+10000)}, \tag{31}$$

and then used as a feedback signal for comparison with the zero reference current. What is left is to design a current controller. A repetitive controller is used here, as shown in Fig. 5. The repetitive controller consists of a proportional controller K_r and an internal model given by

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}}, \tag{32}$$

where τ_d is designed based on the analysis in [1], [20], [21] as $\tau_d = \tau - \frac{1}{\omega_i} = 0.0196\,\text{s}$ with $\omega_i = 2550$, $\tau = 0.02\,\text{s}$.

As shown in Fig.5, the output of the repetitive controller is added to the output of the PI voltage controller to form the final duty cycle before sending it to the PWM block. Then, the generated two complementary PWM signals are used to drive the switches Q_3 and Q_4.

V. Selection of Passive Components

The general principle to select passive components is to minimise their usage. There are in total four passive components, i.e., the capacitors C_- and C, the inductors L_g and L_N. The selection of the C_- is discussed in Subsection III-E. The selection of the inductor L_g is very mature in the literature so it is not repeated here. Interested readers can refer to [22].

A. Selection of the Inductor L_N

Along with the switching on and off of Switches Q_3 and Q_4, the current i_L contains switching ripples. The inductor limits the increasing and decreasing speeds of the current. From the viewpoint of limiting switching current ripples, the inductor should be as large as possible. However, it is preferable to have a small inductor in order to reduce costs and to improve power density and dynamic response.

The operation of the neutral leg is similar to that of a DC/DC buck converter. Switches Q_3 and Q_4 are operated complementarily, the on time of Q_4 is $\frac{d_4}{f_s}$ and the on time of Q_3 is $\frac{1-d_4}{f_s}$ in one PWM period, where f_s is the switching frequency. Since the switching frequency is much higher than the line frequency, it can be assumed that the current increased and decreased are the same during the two modes. Following [17], the peak-peak current ripple can be found as

$$\triangle i_L = \frac{V_+ V_-}{L_N f_s V_{DC}}. \tag{33}$$

As a result, the maximum peak-peak current ripple $\triangle i_{Lm}$ on the inductor L_N is

$$\triangle i_{Lm} = \frac{(V_+ V_-)_{max}}{L_N f_s V_{DC}} \tag{34}$$

where $(V_+V_-)_{max}$ is the maximum value of the product of V_+ and V_-. Since $V_+ + V_- = V_{DC}$, the V_+V_- reaches its maximum value when $V_+ = V_- = \frac{V_{DC}}{2}$. In order to maintain the current ripple less than a given value $\triangle i_{Lm}$, the required minimum inductor is

$$L_{Nmin} = \frac{V_{DC}}{4 f_s \triangle i_{Lm}}. \tag{35}$$

The inductor can be very small if f_s is high enough.

B. Selection of the Capacitor C

Since the low frequencies (both fundamental and second-order) ripples are diverted away from the capacitor C, it is now mainly used to filter output switching ripples, which come from both the conversion leg and the neutral leg. Because the grid current should not have large switching ripples, the level of the switching ripples flowing through the capacitor C is more or less the same as that of the switching ripples flowing through the neutral leg, i.e. the switching ripples flowing through the inductor L_N. According to [23], the peak-peak switching voltage ripples across the capacitor C are

$$\triangle V_{DCs} = \frac{V_{DC}}{32 C L_N f_s^2}. \tag{36}$$

Hence, the required DC-bus capacitor C to meet a given DC-bus voltage ripple $\triangle V_{DCs}$ is

$$C = \frac{V_{DC}}{32 \triangle V_{DCs} L_N f_s^2}. \tag{37}$$

In this paper, only the effect of the switching ripples is considered when choosing the capacitor C. However, the chosen C should be large enough to fulfil the other system requirements, such as hold-up time and dynamic response, for certain applications [16].

C. Design Example

A numerical example is given here with the parameters of the system chosen as $V_g = 110\sqrt{2}$ V, $f = 50$ Hz, $L_g = 2.2$ mH, $L_N = 2.2$ mH, $C = 20$ μF, $C_- = 30$ μF, $R = 690\,\Omega$, $V_{DC}^* = 400$ V and switching frequency $f_s = 19$ kHz. These parameters are taken from the experimental test rig to be validated later.

According to (20), the required minimum capacitance is $C_{-min} = \frac{V_g I_g}{\omega(V_{-max}^2 - V_{-min}^2)} = \frac{\sqrt{2}\times 110\times 3.5}{100\pi(275^2-110^2)} \approx 27$ μF. Here $I_g = 3.5$ A is used to take into account the power losses. The capacitor is then selected as $C_- = 30$ μF to leave some margin. The selection of the inductor L_N mainly depends on its capability to limit switching current ripples. Based on (35), the required minimum inductor is $L_{Nmin} = \frac{V_{DC}}{4 f_s \triangle i_{Lm}} \approx 2$ mH for $\triangle i_{Lm} = 2.5$ A. Here, a 2.2 mH inductor is used. For the DC-bus capacitor $C = 20$ μF, the switching ripple is about $\triangle V_{DCs} = \frac{V_{DC}}{32 C L_N f_s^2} \approx 0.8$ V.

D. Reduction Ratio of the Total Capacitance Required

In order to clearly show the reduction of the total capacitance, a comparison of the required capacitors is made below, to achieve the same level of DC-bus voltage ripples.

Note that V_{DC0} is equal to V_{DC} because the DC-bus voltage ripples are almost eliminated. Taking into account (6), the reduction ratio of the required capacitance of the proposed converter compared to that of the full-bridge converter is

$$r = \frac{2\triangle V_{DC} V_{DC}}{V_{-max}^2 - V_{-min}^2} + \frac{\omega \triangle V_{DC} V_{DC}^2}{16 \triangle V_{DCs} L_N f_s^2 V_g I_g}. \qquad (38)$$

For the numerical example given before, when $\triangle V_{DC} = 5$ V, $r \approx 0.1$ and the required capacitance is reduced by about 10 times. If $\triangle V_{DC} = 2$ V, then $r \approx 0.045$, which means the required capacitance is reduced by about 22 times.

VI. Impact of Adding the Auxiliary Capacitor C_-

In this section, the impact of the auxiliary capacitor is analysed in detail from several aspects, such as the regulation of the DC-bus voltage and the grid current, the voltage stress of the power switches. In order to facilitate the following analysis, a subscript $_f$ is added to the corresponding components/variables of the conventional full-bridge converter.

A. Impact on the Range of the DC-bus Voltage

In order to satisfy $0 \leqslant d_2 \leqslant 1$, according to (9), there is $V_{DC} \geqslant 2V_g$. In other words, the minimum DC-bus voltage should be at least twice of the peak grid voltage V_g. This is the same as conventional half-bridge converters and twice of conventional full-bridge converters. Hence, the topology is particularly good for applications that requires high voltage ratio between the DC side and the AC side, e.g., single-phase to three-phase power conversion [24].

For the same load voltage $V_{DC} = V_{fDC}$, the proposed converter only requires half of the peak grid voltage V_g needed by full-bridge converters. For some applications where a transformer is needed to step down the supply voltage, the transformer used in the proposed converter is smaller and cheaper than that used in full-bridge converter, which improves the system efficiency and the power density.

B. Impact on the Regulation of the Grid Current

The regulation of the grid current mainly depends on the conversion leg. Due to the auxiliary capacitor, the duty cycle is changed from $d_{f2} = 1 - \frac{V_g}{V_{fDC}}|\sin\omega t|$ to $d_2 = \frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}}\sin\omega t$. As a result, the duty cycle is different in order to achieve the same grid current. However, since $0 \leqslant d_2 \leqslant 1$ is always achievable, the grid current can be regulated as usual and hence, is not affected by the addition of the capacitor C_-.

C. Impact on the Current Stress of the Switches

When selecting switches, the average currents are very important [17]. Instead of individually calculating currents flowing through each switch, the sum of the average currents carried by two switches in the same leg is evaluated, which is enough to select switches and design heat dissipation system for the corresponding leg. For the proposed and conventional converter, the current stress of switches is compared in the sequel. In order to facilitate the comparison, a subscription $_f$ is added to the variables, e.g., i_g, V_g, V_-, V_{DC}, Q_1, Q_2, Q_3 and Q_4, for the conventional full-bridge converter. Both peak and RMS values of average currents carried by each leg are calculated for the comparison.

1) Switches of the conversion leg: For the conversion leg, there are two switches, i.e., Q_1 and Q_2. The sum of the currents flowing through the two switches is the grid current. The peak and RMS values of the grid current are I_g and $\frac{I_g}{\sqrt{2}}$, respectively, for the proposed converter, and I_{gf} and $\frac{I_{gf}}{\sqrt{2}}$, respectively, for the conventional converter. If the grid voltage is the same, then $I_g = I_{gf}$, which means the current stress of the switches Q_1 and Q_2 in the two converters are at the same level. However, if the grid voltage is different, then the ratio between the currents carried by the conversion leg in the proposed and the conventional converters is $\frac{V_{gf}}{V_g}$. Since the utilised grid voltage in the proposed converter is half compared to full-bridge converters, then it is possible that, for extreme cases, the grid current in the proposed converter is doubled, i.e., $\frac{i_g}{i_{gf}} = \frac{V_{gf}}{V_g} = 2$. Based on the above analysis, it is clear that the proposed converter is more suitable for applications that requires at least 2 times voltage ratio between the DC side and the AC side, e.g., single-phase to three-phase power conversion [Universal_active_filter].

2) Switches of the neutral leg: For the neutral leg, there are also two switches, i.e., Q_3 and Q_4. The current flowing through the neutral leg depends on the current carried by the inductor L_N. In the conventional converter, the inductor current $i_{Lf} = i_{gf}$. As a result, the peak and RMS values of this current are I_{gf} and $\frac{I_{gf}}{\sqrt{2}}$, respectively. In the proposed converter, according to (16), the peak value of the current i_L is $I_g + \frac{V_g I_g}{2V_-}$. Because $V_g < V_-$, there is

$$I_g + \frac{V_g I_g}{2V_-} \quad < \quad \frac{3}{2} I_g. \qquad (39)$$

As a result, the peak value of the current flowing through the neutral leg in the proposed converter is 1.5 times of that in the conventional full-bridge converter if $I_g = I_{gf}$.

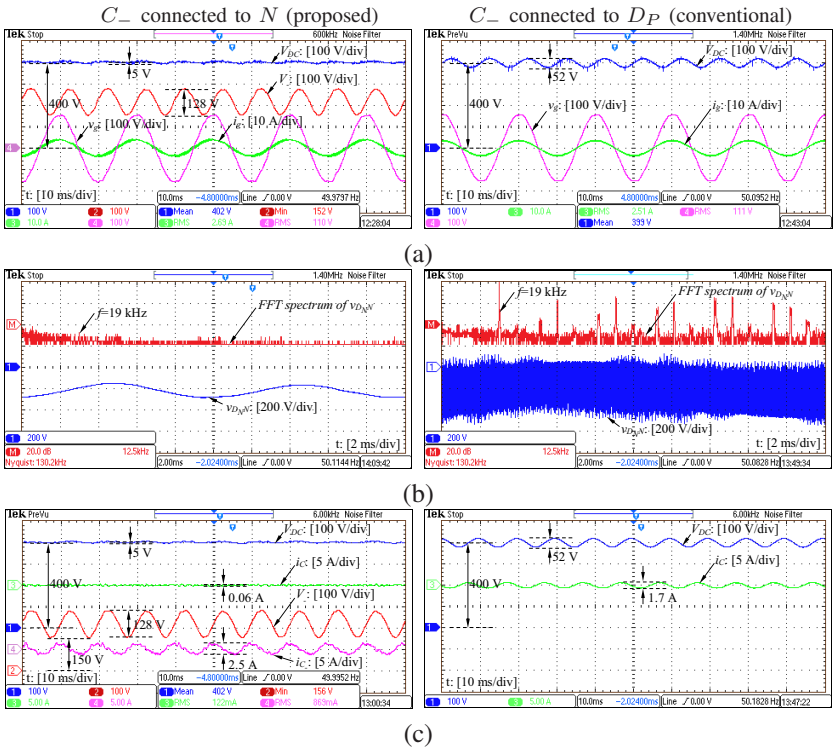


Fig. 6. Experimental results at the steady state (rectification mode): (a) Voltages V_{DC} and V_-, grid voltage v_g and current i_g; (b) CM voltage v_{DNN} and its spectra; (c) DC voltages V_{DC} and V_-, capacitor currents i_C and i_{C-} after applying a 6 kHz low-pass filter.

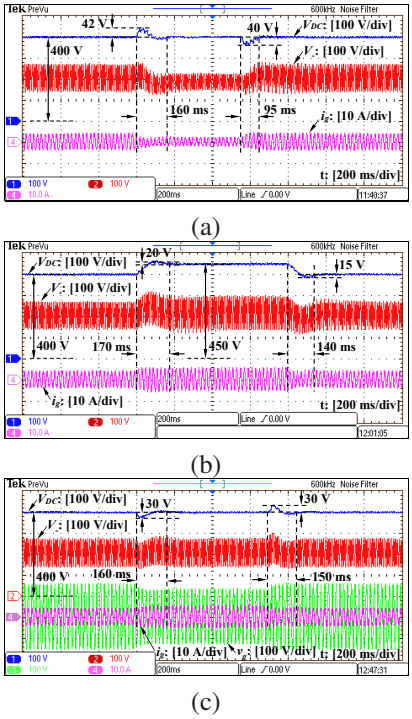


Fig. 7. Transient response in the rectification mode: (a) to a step load change; (b) to a step change of the reference V_{DC}; (c) to a step change of the grid voltage.

At the same time, the RMS value of the i_L can be found as

$$I_L = \sqrt{\frac{I_g^2}{2}(1 + \frac{V_g^2}{2V_-^2})} \tag{40}$$

Again because $V_g < V_-$, there is

$$I_L < \sqrt{\frac{I_g^2}{2}\frac{3}{2}} = \sqrt{\frac{3}{2}}\frac{I_g}{\sqrt{2}} \approx 1.06\frac{I_g}{\sqrt{2}}. \tag{41}$$

Clearly, the RMS value of the i_L in the proposed converter is about 1.06 times of that in the conventional converter if $I_g = I_{gf}$. The higher peak and RMS values are caused by the additional second-order component $\frac{V_g I_g}{2V_-}\cos 2\omega t$, which is diverted from the DC-bus capacitors to reduce DC-bus voltage ripples. As a tradeoff of smoothed voltage ripples, the switches for the neutral leg are under slightly higher current stress.

D. Impact on the Voltage Stress of the Switches

For the switches of conventional full-bridge converters and half-bridge converters, the maximum voltage across the switches is V_{fDC}. Similarly, the maximum voltage across the switches in the proposed converter is V_{DC}. For the same load voltage, i.e. with $V_{DC} = V_{fDC}$, the maximum voltage on the switches are not affected after adding the auxiliary capacitor.

If the same load voltage V_{DC} is applied to the proposed converter and the converter presented in [14], the voltage rating of the switches in the proposed converter can be much lower. In detail, the maximum voltage of switches in the proposed converter is V_{DC} while it is $V_{DC} + V_-$ in [14]. The level of the V_- in [14] is normally set to a high value to tolerate large voltage ripples, which makes the $V_{DC} + V_-$ very high.

VII. Experimental Validation

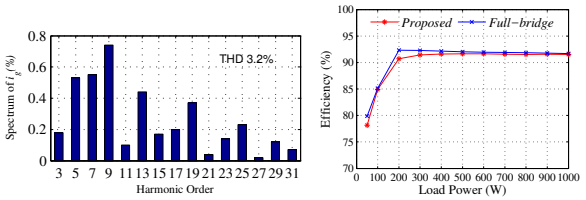
In order to validate the proposed converter, a test rig was assembled in the lab. The system parameters are the same as the ones used in the numerical example. The capacitors used are one 20 μF metallized polypropylene film capacitor for C and one 30 μF for C_-, respectively.

A. Operation in the Rectification Mode

1) Steady-state performance: In order to demonstrate the performance improvement of adding the auxiliary capacitor, the experiments were carried out for two cases: one for the proposed topology with C_- connected to the neutral point N with $V_{-min}^* = 150$ V and the other for the conventional full-bridge with C_- connected to the positive pole D_P of the DC bus (in parallel with C). The reference of the DC-bus voltage V_{DC} is set at 400 V for both cases, which is slightly higher than the required voltage $2V_g$, and a resistive load 690 Ω is connected across the DC bus. For the proposed topology, V_{-min} is set at 150 V. The results are shown in Fig. 6. The DC-bus voltage V_{DC} for the proposed topology is maintained very well around its reference with very low voltage ripples (around 5 V). However, the conventional full-bridge converter has very high voltage ripples (around 52 V). For the proposed topology, the voltage V_- across the capacitor C_- has high voltage ripples, at around 128 V, as designed. Because of the allowable large voltage ripples, the auxiliary capacitor C_- can be small and hence the total capacitance is reduced significantly. Alternatively, with the same total capacitance, the DC-bus voltage ripples are reduced by 90%.

Apart from having low output voltage ripples, it is also important to have a clean grid current, which is also in phase

with the grid voltage to achieve the unity power factor. As shown in Fig. 6(a), the grid current is well regulated to be in phase with the grid voltage for both cases. According to the experimental data, the power factor is above 0.99. Note that no special efforts are made to improve the power quality of the test rig and, hence, the quality of the i_g is very good. For the conventional full-bridge converter, the THD of the i_g is 3.2%, which is comparable to that of the proposed converter.



(a) (b)

Fig. 8. System performance: (a) harmonic spectrum of the grid current i_g; (b) efficiency comparison.

For both converters, the CM voltage $v_{D_N N}$ between the DC ground D_N and the AC ground N was measured and the results are shown in 6(b). Also, the FFT spectra of the CM voltages are shown in 6(b). Obviously, the high-frequency components in $v_{D_N N}$, which contribute to most of leakage currents, are significantly reduced in the proposed converter with comparison to the conventional bridge converter.

In order to demonstrate how the ripple power is diverted from C to C_-, the corresponding capacitor current i_C and i_{C-} are shown in Fig. 6(c) after applying a filter having a bandwidth of 6 kHz to filter out the switching ripples. For the proposed converter, the current i_C is around 0.06 A without visible low-frequency components and hence, the output voltage V_{DC} is almost ripple-free. For the conventional bridge converter, the i_C is around 1.7 A because most of the second-order current flows through the DC-bus capacitors. On the other hand, the second-order harmonic current in the proposed converter is diverted to the C_-, as expected, and the i_{C-} has relatively large ripples as designed, at 2.5 A.

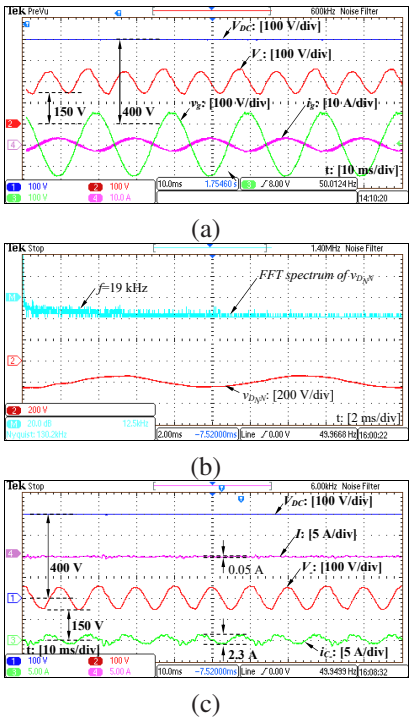
According to the recorded experimental data, the harmonic spectrum of the grid current i_g is shown in Fig. 8(a). Clearly, the total harmonic distortion (THD) of the grid current is around 3%, which is already very low because no special efforts, e.g., optimization of filters, are made to improve the power quality of the grid current.

2) Transient performance: Fig. 7 shows the transient performance of the proposed converter under three scenarios. The first one is a step load change. As seen in Fig. 7(a), the system only took at about 160 ms (8 fundamental cycles) and 95 ms (less than 5 fundamental cycles), respectively, for a step load change from the full load (690 Ω) to 50% load (1380 Ω), and back to the full load (690 Ω).

As shown in Fig. 7(b), the second scenario is a step change of the reference V_{DC} from 400 V to 450 V, and back to 400 V. The transient process took about 170 ms from 400 V to 450 V and took about 140 ms from 450 V to 400 V.

Fig. 7(c) shows the waveforms of the proposed converter for the third scenario with a step decrease and then increase of the grid voltage for about 20 V. Clearly, the DC-bus voltage V_{DC} can be well maintained around its reference even during a step change of the grid voltage. Note that the grid current was also controlled well without noticeable spikes, which indicates the good transient performance of the controllers.

During the aforementioned three transient scenarios, it is worth highlighting that the ripple of the V_{DC} is always maintained at about 5 V, which is important for the operated DC loads. As expected, the ripple of the V_- is increased if the system power is increased while it is decreased if the system power is lowered, as shown in Fig. 7(a) and (b).



(a)

(b)

(c)

Fig. 9. Experimental results (inversion mode): (a) Voltages V_{DC} and V_-, grid voltage v_g and current i_g; (b) CM voltage $v_{D_N N}$ and its spectra; (c) Voltages V_{DC} and V_-, DC-bus current I and capacitor current i_{C-} after applying a 6 kHz low-pass filter to remove the switching ripples.

3) Efficiency: In order to evaluate the performance of the proposed system on efficiency, an efficiency comparison using PLECS was made, between the proposed converter with C_- connected to the neutral point N and the conventional full-bridge converter with C_- connected to the positive pole D_P of the DC bus (in parallel with C). The systems were tested from 50 W to 1000 W by changing the DC load R. Note that the DC-bus voltage is always kept at 400 V. The obtained results are shown in Fig. 8(b). The efficiency of the proposed converter is comparable to that of the conventional full-bridge converter when the power is high. Normally, an isolation transformer is required in conventional full-bridge converters to reduce CM voltage, which introduces about 2% efficiency drop [2]. At the same time, if an active filter is used to reduce DC-bus voltage ripples in a full-bridge converter, the system efficiency could drop by about 3% [25]. As a result, the efficiency of the proposed converter is likely to be higher than that of a full-bridge converter having a transformer and an active filter.

B. Operation in the Inversion Mode

In order to demonstrate the operation of the proposed converter as an inverter, a DC voltage source instead of a load

is connected across the DC bus (the AC side of the system is still connected to the grid). The output voltage of the DC source is set at $400\,\mathrm{V}$. In addition, the controller of the neutral leg is kept to be the same while the following changes are made on the controller of the conversion leg to control the power sent to the grid: (1) The PI controller for the DC-bus voltage is removed but the repetitive controller for the grid current is kept; (2) The reference of the grid current is set as $I_g^* = -3\sin\omega t$ in experiments.

The corresponding waveforms of the proposed system are shown in Fig. 9 when operated as an inverter. It is clear that the proposed system can be operated in the inversion mode without any problem. For example, as shown in Fig. 9(a), the grid current is well controlled with 180° phase difference with the grid voltage, which means the proposed system is indeed operated as inverter to send the power from the DC power source to the grid. According to the recorded experimental data, the grid current has low THD (around 4%) and high power factor (above 0.99). Additionally, high-frequency components in v_{D_NN} are almost eliminated according to the spectrum of the CM voltage shown in 9(b), which contribute to most of leakage currents. Importantly, the DC-bus current I is controlled to have very low ripples and most of the ripple energy is again diverted to the capacitor C_-, which makes the current i_{C_-} contains noticeable ripple components as shown in Fig. 9(c).

VIII. Conclusions

An auxiliary capacitor has been added to the widely-used full-bridge converters with four switches, which has resulted in significantly-reduced leakage currents, DC-bus voltage ripples and, at the same time, total capacitance needed. Because of the added auxiliary capacitor, the operation of the converter is very different from that of the conventional full-bridge converters. The two legs are operated independently from each other, which makes the design of both legs very flexible. One leg remains to take the responsibility of exchanging energy with the grid to achieve unity power factor and to regulate the DC-bus voltage; the other leg is to divert the ripple energy from the DC-bus capacitor to the auxiliary capacitor. Although the number of capacitors is increased from one to two, it has been demonstrated that the total capacitance needed becomes much smaller, which makes it possible to replace bulky electrolytic capacitors with film capacitors to improve power density and reliability. Extensive experimental results for both rectification and inversion modes have validated the high performance of the proposed converter, with comparison to the conventional full-bridge converter having the same parameters.

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